Amendments to the Claims:

None of the claims have been amended herein. All of the pending claims 1-29 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as previously amended.

Listing of Claims:

1. (Previously presented) A method for forming a semiconductor device assembly, comprising:

providing a carrier substrate including at least one die-attach location and at least one terminal adjacent to the at least one die-attach location; and

providing a solder mask on the carrier substrate, the solder mask including at least one device-securing region positioned over at least a portion of the at least one die-attach location, at least one recessed area adjacent to the at least one device-securing region, and at least one dam adjacent to the at least one recessed area, opposite from the at least one device-securing region, the at least one dam contacting at least a portion of a peripheral edge of the at least one terminal.

2. (Previously presented) The method of claim 1, further comprising:

applying adhesive material to at least one of the at least one device-securing region of the solder mask and a bottom surface of at least one semiconductor device to be secured to the at least one device-securing region.

3. (Previously presented) The method of claim 2, further comprising:

positioning the at least one semiconductor device on the at least one device-securing region, the adhesive material located between the bottom surface and the at least one device-securing region securing the at least one semiconductor device to the at least one device-securing region.

4. (Previously presented) The method of claim 3, wherein positioning comprises applying force to at least one of the at least one semiconductor device and the carrier substrate.

5. (Previously presented) The method of claim 3, wherein positioning comprises forcing the adhesive material to spread between the bottom surface of the at least one semiconductor device and the at least one device-securing region.

6. (Previously presented) The method of claim 5, wherein positioning comprises causing excess adhesive material to flow laterally beyond at least one of a peripheral edge of the at least one semiconductor device and a periphery of the at least one device-securing region.

7. (Previously presented) The method of claim 6, further comprising:
receiving the excess adhesive material within the at least one recessed area.

8. (Previously presented) The method of claim 6, wherein the at least one dam prevents the excess adhesive material from contaminating a connection surface of the at least one terminal.

9. (Previously presented) The method of claim 1, wherein providing the solder mask comprises providing a solder mask with the at least one dam comprising a laterally extending portion configured to cover at least portion of a peripheral edge of a connection surface of the at least one terminal.

10. (Previously presented) The method of claim 1, wherein providing the solder mask comprises providing the carrier substrate with the solder mask already secured thereto.

11. (Previously presented) The method of claim 1, wherein providing the solder mask includes securing a preformed solder mask to a surface of the carrier substrate.

12. (Previously presented) The method of claim 1, wherein providing the solder mask includes forming the solder mask on a surface of the carrier substrate.

13. (Previously presented) The method of claim 12, wherein forming is effected stereolithographically.

14. (Previously presented) The method of claim 12, wherein forming comprises forming a plurality of at least partially superimposed, contiguous, mutually adhered material layers.

15. (Previously presented) A method for designing a solder mask for use on a carrier substrate, comprising:

configuring at least one device-securing region to have a semiconductor device secured thereto; and

configuring a plurality of raised dams to be positioned adjacent to and in contact with peripheries of terminals of the carrier substrate.

16. (Previously presented) The method of claim 15, further comprising:

configuring at least one recessed area between at least a portion of a periphery of the at least one device-securing region and at least one of the plurality of raised dams.

17. (Previously presented) A method for designing a solder mask for use on a carrier substrate, comprising:

configuring at least one device-securing region to have a semiconductor device secured thereto; and

configuring at least one recessed area adjacent to the at least one device-securing region.

18. (Previously presented) The method of claim 17, further comprising:

configuring a plurality of raised dams adjacent to the at least one recessed area, opposite from the at least one device-securing region.

19. (Previously presented) A method for designing a solder mask to be used on a carrier substrate, comprising:

configuring at least one device-securing region of the solder mask to be located over at least a portion of a die-attach location of the carrier substrate;

configuring at least one recessed area laterally adjacent to the at least one device-securing region; and

configuring at least one dam adjacent to the at least one recessed area, opposite from the at least one device-securing region, to be located laterally adjacent to and contact a peripheral edge of a terminal protruding from a surface of the carrier substrate, and to have a height at least as great as a height of the at least one device-securing region.

20. (Previously presented) The method of claim 19, wherein configuring the at least one dam comprises configuring the at least one dam to include a laterally extending ledge positionable over at least a portion of a peripheral edge of a connection surface of the terminal.

21. (Previously presented) The method of claim 19, wherein configuring the at least one dam comprises configuring the at least one dam to have a height that exceeds the height of the at least one device-securing region.

22. (Previously presented) The method of claim 21, wherein configuring the at least one dam comprises configuring the at least one dam to be located at an elevation which is substantially the same as or less than an elevation of an active surface of a semiconductor device to be positioned on the at least one device-securing region.

23. (Previously presented) A method for designing a carrier substrate, comprising:

configuring a substantially planar substrate to include at least one die-attach location; and

configuring at least one terminal adjacent to the at least one die-attach location and to protrude a sufficient distance from the substantially planar substrate to prevent excess adhesive material forced from between a semiconductor device and the at least one die-attach location from contaminating a connection surface of the at least one terminal.

24. (Previously presented) The method of claim 23, further comprising: configuring an adhesive-receiving area between the at least one die-attach location and the at least one terminal.

25. (Previously presented) The method of claim 24, wherein configuring the adhesive-receiving area comprises configuring at least one recess.

26. (Previously presented) The method of claim 25, wherein configuring at least one recess comprises configuring the at least one recess to substantially laterally surround the at least one die-attach location.

27. (Previously presented) The method of claim 25, wherein configuring at least one recess comprises configuring the at least one recess to be located adjacent to only a portion of the at least one die-attach location.

28. (Previously presented) The method of claim 23, wherein configuring the at least one terminal comprises configuring the at least one terminal to have a height that is at least as great as an elevation at which a bottom surface of the semiconductor device will be supported above a surface of the substantially planar substrate.

29. (Previously presented) The method of claim 28, wherein configuring the at least one terminal comprises configuring the at least one terminal to have a height that is, at most, substantially the same as an elevation at which a top surface of the semiconductor device will be located upon securing the semiconductor device relative to the substantially planar substrate.